IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): Daubenspeck, *et al.*

Examiner: Dang, Trung Q.

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Title: **CHIP DICING**

Commissioner for Patents
P.O. Box 1450
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Do not Enter
T. Dang
7/19/06

REQUEST FOR RECONSIDERATION

Sir:

This Request for Reconsideration is in response to the Office Action mailed April 19, 2006.

In the Claims:

Please amend claims 3 and 5. Please cancel claims 1, 2, 4, and 7. The claims are as follows:

1. (Canceled).

2. (Canceled).

3. (Currently amended) ~~The method of claim 1~~ A method for chip separation, the method comprising the steps of:

(a) providing a semiconductor substrate;

(b) forming first and second device regions in and at top of the semiconductor substrate,

wherein the first and second device regions are separated by a semiconductor border region of the semiconductor substrate;

(c) forming N interconnect layers, in turn, directly above the semiconductor border region and the first and second device regions,

wherein N is a positive integer greater than one,

wherein each layer of the N interconnect layers comprises an etchable portion directly

above the semiconductor border region,

wherein the etchable portions of the N interconnect layers form a continuous etchable block directly above the semiconductor border region, and

wherein the entire continuous etchable block comprises essentially a same material throughout the entire continuous etchable block;

(d) removing the continuous etchable block by etching; and

(e) cutting with a laser through the semiconductor border region via an empty space of the removed continuous etchable block, wherein the continuous etchable block comprises copper.

4. (Canceled).

5. (Currently amended) ~~The method of claim 1, further comprising the steps of:~~ A method for chip separation, the method comprising the steps of:

(a) providing a semiconductor substrate;

(b) forming first and second device regions in and at top of the semiconductor substrate,

wherein the first and second device regions are separated by a semiconductor border region of the semiconductor substrate;

(c) forming N interconnect layers, in turn, directly above the semiconductor border region and the first and second device regions,

wherein N is a positive integer greater than one,

wherein each layer of the N interconnect layers comprises an etchable portion directly above the semiconductor border region,

wherein the etchable portions of the N interconnect layers form a continuous etchable block directly above the semiconductor border region, and

wherein the entire continuous etchable block comprises essentially a same material throughout the entire continuous etchable block;

(d) removing the continuous etchable block by etching;

(e) cutting with a laser through the semiconductor border region via an empty space of the removed continuous etchable block;

(f) back-side grinding a back surface of the semiconductor substrate; and then

(g) applying a dicing tape to the back surface of the semiconductor substrate before the step of removing the continuous etchable block by etching.

6. (Previously presented) A method for chip separation, the method comprising the steps of:

(a) providing a semiconductor substrate;

(b) forming first and second device regions in and at top of the semiconductor substrate,

wherein the first and second device regions are separated by a semiconductor border region of the semiconductor substrate;

(c) forming N interconnect layers, in turn, directly above the semiconductor border region and the first and second device regions,

wherein N is a positive integer greater than one,

wherein each layer of the N interconnect layers comprises an etchable portion directly above the semiconductor border region,

wherein the etchable portions of the N interconnect layers form a continuous etchable block directly above the semiconductor border region, and

wherein the entire continuous etchable block comprises essentially a same material;

(d) removing the continuous etchable block by etching; and

(e) cutting with a laser through the semiconductor border region via an empty space of the removed continuous etchable block,

wherein the semiconductor substrate comprises bulk silicon, and

wherein, after the step of removing the continuous etchable block by etching, but before

the step of cutting by the laser through the semiconductor border region, the method further comprises the step of wet etching a portion of the semiconductor border region so as to form a V-shaped trench in the semiconductor border region.

7. (Canceled).

8. (Previously presented) A method for chip separation, the method comprising the steps of:

(a) providing a semiconductor substrate;

(b) forming first and second device regions in and at top of the semiconductor substrate,

wherein the first and second device regions are separated by a semiconductor border region of the semiconductor substrate;

(c) forming N interconnect layers, in turn, directly above the semiconductor border region and the first and second device regions,

wherein N is a positive integer greater than one,

wherein each layer of the N interconnect layers comprises an etchable portion directly above the semiconductor border region,

wherein the etchable portions of the N interconnect layers form a continuous etchable

block directly above the semiconductor border region, and

wherein the entire continuous etchable block comprises essentially a same material;

(d) removing the continuous etchable block by etching; and

(e) cutting with a laser through the semiconductor border region via an empty space of the removed continuous etchable block,

wherein each layer of the N interconnect layers further comprises first and second chip edge portions and first and second isolation portions directly above the semiconductor border region, and

wherein the first chip edge portions of the N interconnect layers form a first continuous chip edge block directly above the semiconductor border region,

wherein the second chip edge portions of the N interconnect layers form a second continuous chip edge block directly above the semiconductor border region,

wherein the first isolation portions of the N interconnect layers form a first continuous isolation block directly above the semiconductor border region,

wherein the second isolation portions of the N interconnect layers form a second continuous isolation block directly above the semiconductor border region,

wherein the continuous etchable block is sandwiched between the first and second continuous isolation blocks,

wherein the first continuous isolation block is sandwiched between the continuous etchable block and the first continuous chip edge block,

wherein the second continuous isolation block is sandwiched between the continuous etchable block and the second continuous chip edge block, and

wherein the first and second isolation portions comprise a material which is essentially not affected by the step of removing the continuous etchable block by etching.

9. (Original) The method of claim 8, wherein the first and second continuous chip edge blocks comprise a same material as the continuous etchable block.

10. (Original) The method of claim 9, wherein the same material of the first and second continuous chip edge blocks and the continuous etchable block comprises copper.

11. (Original) The method of claim 8, wherein the first and second continuous chip edge blocks comprise a material that is essentially not affected by the laser.

12. (Previously presented) A method for chip separation, the method comprising the steps of:

(a) providing a semiconductor substrate;

(b) forming first and second device regions and a filled deep trench in and at top of the semiconductor substrate,

wherein the first and second device regions are separated by a semiconductor border region of the semiconductor substrate, and

wherein the semiconductor border region comprises the filled deep trench;

(c) forming N interconnect layers, in turn, directly above the border region and the first and second device regions,

wherein N is a positive integer greater than one,

wherein each layer of the N interconnect layers comprises an etchable portion directly above the filled deep trench,

wherein the etchable portions of the N interconnect layers form a continuous etchable block directly above the filled deep trench, and

wherein the entire continuous etchable block comprises essentially a same material throughout the entire continuous etchable block;

(d) removing the continuous etchable block by etching; and

(e) cutting with a laser through the filled deep trench via an empty space of the removed continuous etchable block.

13. (Original) The method of claim 12, wherein the filled deep trench comprises a material which can be easily cut through by the laser.

14. (Original) The method of claim 12, wherein the filled deep trench comprises a material selected from the group consisting of polysilicon and silicon oxide.

15. (Withdrawn) A semiconductor structure, comprising:

(a) first and second device regions in and at top of a semiconductor substrate, wherein the first and second device regions are separated by a semiconductor border region of the semiconductor substrate; and

(b) N interconnect layers directly above the border region and the first and second device regions,

wherein N is a positive integer,

wherein each layer of the N interconnect layers comprises an etchable portion directly above the semiconductor border region, and

wherein the etchable portions of the N interconnect layers form a continuous etchable block directly above the semiconductor border region.

16. (Withdrawn) The structure of claim 15, wherein the continuous etchable block comprises a material which is etchable by wet etching.

17. (Withdrawn) The structure of claim 15, wherein the continuous etchable block comprises copper.

18. (Withdrawn) The structure of claim 15,

wherein each layer of the N interconnect layers further comprises first and second chip edge portions and first and second isolation portions directly above the semiconductor border region, and

wherein the first chip edge portions of the N interconnect layers form a first continuous chip edge block directly above the semiconductor border region,

wherein the second chip edge portions of the N interconnect layers form a second continuous chip edge block directly above the semiconductor border region,

wherein the first isolation portions of the N interconnect layers form a first continuous isolation block directly above the semiconductor border region,

wherein the second isolation portions of the N interconnect layers form a second

continuous isolation block directly above the semiconductor border region,

wherein the continuous etchable block is sandwiched between the first and second continuous isolation blocks,

wherein the first continuous isolation block is sandwiched between the continuous etchable block and the first continuous chip edge block, and

wherein the second continuous isolation block is sandwiched between the continuous etchable block and the second continuous chip edge block.

19. (Withdrawn) The structure of claim 18, wherein the first and second continuous chip edge blocks comprise a same material as the continuous etchable block.

20. (Withdrawn) The method of claim 19, wherein the same material of the first and second continuous chip edge blocks and the continuous etchable block comprises copper.

REMARKS

The Examiner allowed claims 6 and 8-14. Applicants gratefully acknowledge the Examiner's indication of allowed subject matter.

The Examiner objected to claims 3 and 5 as being dependent upon rejected base claim 1, but would be allowable if rewritten in independent form including all of the limitations of the base claim 1 and any intervening claims. Accordingly, Applicants have rewritten claims 3 and 5 in independent form including all of the limitations of the base claim 1.

The Examiner rejected claims 1 and 7 under 35 U.S.C. § 102(e) as allegedly being anticipated by Takao (US 2004/0137701). In response, Applicants have canceled claims 1 and 7.

The Examiner rejected claims 2 and 4 under 35 U.S.C. § 103(a) as allegedly being unpatentable over Takao as above in view of Chae *et al.* (US 6,958,312). In response, Applicants have canceled claims 2 and 4.

In short, Applicants have (i) rewritten all objected-to claims 3 and 5 in independent form including all of the limitations of the base claim 1, and (ii) canceled all rejected claims 1, 2, 4, and 7.

CONCLUSION

Based on the preceding amendments, Applicants respectfully believe that all pending claims and the entire application meet the acceptance criteria for allowance and therefore request favorable action. If the Examiner believes that anything further would be helpful to place the application in better condition for allowance, Applicants invites the Examiner to contact Applicant's representative at the telephone number listed below. The Director is hereby authorized to charge and/or credit Deposit Account 09-0456.

Date: 07/17/2006

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